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(54) Switching voltage regulator, having a driver circuit of a power MOS switch

(57) The invention relates to a switching voltage regulator incorporating a driver circuit of a MOS power switch. Advantageously, the MOS switch is formed of a plurality (n) of power transistors (M1, M2, ..., Mn) connected in parallel to each other. In particular, the first (M1) of said plurality of transistors (M1, M2, ..., Mn) has larger sizes (W1) than the other transistors, or better still, the sizes (Wi) of the individual power transistors (M1, M2, ..., Mn) scale down (W1 • W2 ≥ W3 ... ≥ Wn).

In this way, the equivalent dimensional parameter (W) of the power switch is greatly reduced by that the first and largest translator (M1) is readily turned. This is carried out without affecting the delivered current, which continues to be supplied by the remaining transistors (M2, ..., Mn).

Compared to the prior art solutions, this arrangement functions to modify the power switch own tansconductance, which decreases as the transistors are turned off onward from the first (M1).

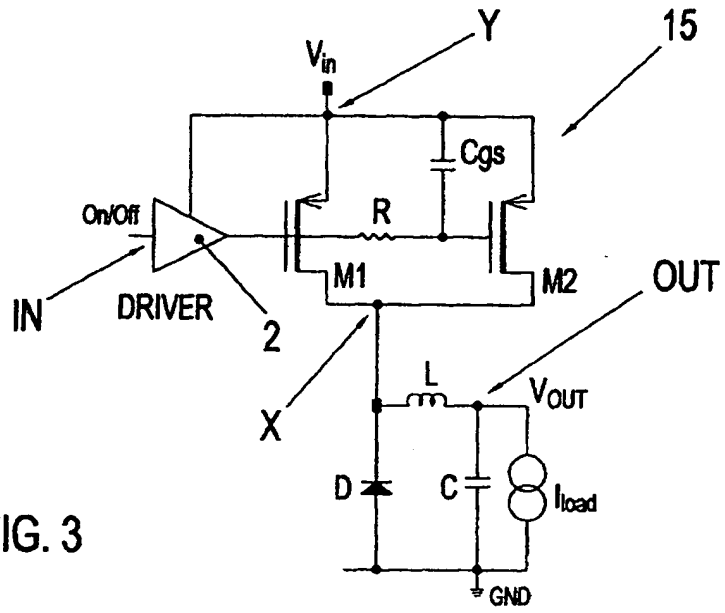

FIG. 3

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Description

DESCRIPTION

Field of the Invention

[0001] This invention relates to a driver circuit for a MOS power switch incorporated in a switching voltage regulator.

[0002] The setting of this invention is the development of a new family of devices fabricated with BCDV technology, specifically a switching voltage regulator of the step-down type which has a plurality of output currents and is associated with a current loop for a battery charger. The following description is made with reference to this technical field for the sake of simplicity only.

[0003] Switching voltage regulators are widely utilized in many applications because of their efficiency and precision features. These regulators include, as their basic components: a transistor-based power switch, a loop-back diode, an LC output filter, and an optional current sensor for the battery charger.

Prior Art

[0004] To be competitive, new-generation regulators must have ever higher switching frequencies, so that ever smaller external components can be employed to fill demands for both reduced circuit apace occupation and enhanced cost efficiency. In particular, these regulators should have the number of their external components reduced to a minimum. The frequency increase implies a limited regulator efficiency mainly because of the switching losses of the power switch. Accordingly, the most critical aspect of the regulator carrying out is its circuit portion devoted to driving the power switch, since switching losses are dependent on that portion.

[0005] One of the problems faced by the driver circuits of such power switches is that of achieving a total reduction of both static and dynamic consumption, as well as a control of the current edges so as to minimize electromagnetic disturbance and avoid spurious operation due to any current limiters becoming activated at power-on.

[0006] Another no less important problem is the power switch stressing caused by the speed of the power on/off edges, and the presence of parasitic RLC circuit portions in the load as well as the device itself. In a specific application, bonding wires and board conduction paths would be connected in series with the source and the drain of the power switch.

[0007] From physics, it is known that an inductor being traversed by a current I would resist a sharp variation in the current by presenting an overvoltage at its heads, which is proportional to the inductance L value and the rate of variation of the current, according to the following relation:

$$\Delta V = L(dI/dt).$$

[0008] In switching voltage regulators, the current flowing through the power switch exhibits variations of several hundreds Amperes per microsecond, both at power-on and power-off phases. The parasitic inductance L of bonding wires may instead be as high as a few tens nH. It follows that, with the current edges being so fast, and because of the values of the parasitic inductance, overvoltages of even 10V may occur at the source and the drain of the power switch.

[0009] If the regulator operates at the highest admissible input voltage, these overvoltages, by adding with one another, can push the power switch transistor outside its SOA (Safe Operating Area), possibly wrecking it by voltage breakdown.

[0010] The phenomenon just described is bound to occur when either an N-channel or a P-channel MOS power transistor is used.

[0011] Figure 1 herein shows, by way of example, the schematic structure of a switching voltage regulator 1 which comprises an N-channel MOS power transistor. The driver circuit 2 of such regulator has been optimized to minimize the effect of the time taken to go through the loop-back diode, and in accordance with the teachings of US Patent No. 5,883,505 to the same Applicant.

[0012] The power-on edge is optimized essentially by having the gate of the power switch slowly charged until the loop-back on the diode D is over. This gate is then charged very fast to minimize switching losses.

[0013] In this type of regulator, the critical switching edge is still the power-off edge, because in order to control the current edge at power-off, it would be necessary to proceed in exactly the opposite way to the power-on situation.

[0014] In fact, in order to slow down the current edge, the power transistor gate would have to be discharged very slowly, and this is unfortunately in conflict with the need of consumption minimization, while also presenting practical difficulties because the power transistor is very large (W of a few tens mm), and when operating close to the threshold value, a few mV variation of the voltage Vgs between the gate and source terminals is enough to produce large variations of the drain Ipower current. The drive voltage of the power transistor should therefore be controlled in a very precise manner (within one mV).

[0015] In other words, to handle the current edge at power-off and at the same time to achieve optimized efficiency, Vgs of the power transistor should be quickly decreased until it nears the threshold value and then should be slowly and accurately varied within one mV. Producing a suitable circuit to fill this demand is practically impossible with current BCD technologies; in fact, components would be needed which can respond within a very short time (a few nanoseconds). And even where such components can be made available, it would be

necessary to have the voltage at the gate terminal varied very slowly and with a very high precision. (A few mV variation can result in a several Ampere variation occurring in the current.)

[0016] The state of the art provides no circuital solutions which can meet both of the aforementioned requirements both at power-on and at power-off. It has been current practice to try to overcome the cited problem by driving the gate terminal of the power transistor very slowly also during the first power-on phase, when this would be unnecessary. Shown in Figure 1A are respective patterns 7, 8 of the Ipower current and of the voltage drop Vds for the circuit of Figure 1, at the power-on and power-off stages thereof.

[0017] This prior solution obviously results in increased switching losses and, hence, poorer overall efficiency of the regulator.

[0018] The underlying technical problem of this invention is to contrive a new type of driver circuit for a power transistor, which circuit exhibits appropriate structural and functional features to afford reliable handling of the overvoltage effects, caused by the speed of the current edges during the switching, thereby to obviate the aforementioned drawbacks with reference to the prior art.

[0019] In essence, the driver circuit of this invention is to ensure the same speed of response at the power-on as at the power-off edges, at the same time minimizing consumption and avoiding to stress the power transistor gate.

Summary of the Invention

[0020] The principle of this invention is the one of providing the power transistor which forms the power switch by means of a plurality of transistors which are connected to each other in parallel and have scaled dimensions so that they can be independently driven.

[0021] Based on this principle, the technical problem is solved by a voltage regulator as defined in Claim 1 foll..

[0022] The features and advantages of a regulator according to this invention will be apparent from the description of an embodiment thereof, given by way of non-limitative example with reference to the accompanying drawings.

[0023] In the drawings:

Brief Description of the Drawings

[0024]

- Figure 1 schematically shows a switching voltage regulator realized according to the prior art.
- Figure 1A shows a diagram reporting, in function of time, the voltage and the current signals present in the regulator of Figure 1.
- Figure 2 shows a schematic view of a switching voltage regulator realized according to the present invention.
- Figure 3 shows a particular embodiment of the regulator of Figure 2.
- Figure 4 shows a diagram reporting, in function of time, the voltage and the current signals present in the regulator of Figure 2 and compared with the signals of the regulator of Figure 1.

Detailed Description

[0025] With reference to the drawings, and particularly to Figure 2 thereof, a switching voltage regulator according to this invention is overall and schematically shown at 10 in schematic form.

[0026] This regulator 10 is connected between a first Vin voltage reference of supply and a second ground reference, and comprises a power switch formed by a MOS-type power transistor driven by a driver circuit 2. The power switch is intended to drive an electric load on a node OUT, and is associated with a current loop illustrated by a circuit LC having a loop-back diode D associated therewith.

[0027] More particularly in this invention, the power switch is formed of a plurality of power transistors M1, M2, Mn-1 Mn which are connected in parallel to each other.

[0028] Essentially, the power switch of the regulator has been split into a plurality of n switches obtained by corresponding power transistors M1, M2,..., Mn which are connected in parallel to each other and are smaller than the single power transistor, which formed the switch of the prior art. More particularly, calling Wtot the width required to obtain the desired internal resistance Ron at power-on conditions, the dimensions Wi of the individual power transistors M1, M2,..., Mn are scaled down such that:

$$Wtot = \Sigma_i^n Wn,$$

and

$$W1 * W2 \geq W3 ... \geq Wn.$$

[0029] The gate terminals of each of then transistors M1, M2,..., Mn are driven by a single driver circuit 2 such that the gate terminal of the largest transistor, M1, is discharged very fast, while the gate terminals of the other transistors, M2,..., Mn-1, Mn, of decreasing size are suitably driven by control circuit portions 4, 5, 6..., which are connected between the output of the driver circuit 2 and each respective gate terminal of the corresponding transistor.

[0030] By employing these control circuit portions 4, 5, 6,.., the size of the power transistors to be driven is allowed to decrease gradually, while also controlling the leading and trailing edges of the current.

[0031] In this way, the equivalent dimensional parameter W of the power switch is greatly reduced because, at power-off, the first transistor M1 with the largest value W1 is readily turned off., All this occurs without affecting the delivered current, since it keeps to be delivered by the remaining transistors M2,..., Mn. Also, with a reduced W, it becomes possible to control, in a finer way and with a wider margin, the edge of the current delivered from the plurality of transistors M1,..., Mn, particularly when approaching the tripping threshold of the whole set of transistors. In fact, the control no longer requires that just a few millivolts be monitored as in the prior art.

[0032] The control circuit portions may be implemented, for example, with appropriate delay blocks. Furthermore, it would be perfectly possible to separately drive the n gate terminals and/or move the control of such terminals to a location upstream of the driver circuit 2.

[0033] Compared to the prior art solutions, with this structure the transconductance of the power switch is modified since it decreases as the transistors are turned off starting with M1, and allows the voltage drop Vgs to be varied faster to obtain the same current edge. This obviously minimizes consumption and optimizes the entire system efficiency.

[0034] This solution overcomes the problems mentioned with reference to the prior art, and can be applied to N-channel as well as to P-channel topologies. The theoretical diagram shown in Figure 2 relates to a P-channel topology, but it would be very easy for a skilled person in the art to adapt the diagram for an N-channel topology.

[0035] Referring to the example shown in Figure 3, a particular embodiment 15 of the inventive regulator will now be described.

[0036] In this example, the power transistor has been split for simplicity's sake into two transistors M1, M2 only. These transistors are connected in parallel to each other between the nodes Y and X, and their dimensions W1 and W2 are in agreement with the following relations:

$$W_{M1} = n \cdot W_{M2},$$

and

$$W_{TOT} = W_{M1} + W_{M2}.$$

[0037] The control circuit portion is essentially formed essentially with a delay block which is implemented by an RC network comprising a resistor R connected between the gate terminals of the transistors M1, M2, and a parasitic capacitor Cgs present between the gate and source terminals of the second power transistor M2. In this way, the larger transistor, M1, is turned off very rapidly while the second transistor M2 keeps delivering the required current to the output circuit LC until the loop-back diode begins conducting. The Vgs voltage drop of the second transistor M2 is slowly decreased (according to an exponential function with a time constant τ=RCgs) in these conditions, since the transconductance of the transistor M2 is small, and by an appropriate selection of n and R, the edge of the current (about 50A/μs) delivered from the transistor M2 can be effectively controlled.

[0038] In the diagram of Figure 4, it is shown a comparison between the current edges I, I1 and the Vds voltage at the heads of the power switch in the case in which said switch is formed with a single transistor (curves 12 and 9) in accordance with the prior art, or with the plurality of paralleled power transistors provided by this invention (curves 13 and 14), the driver circuit 2 being the same in both cases. It can be easily seen that, with the inventive structure, the current power-off edge is controlled such that the drain-source voltage of the power switch will never exceed its SOA limit (40V in the example).

[0039] To achieve the same results by merely slowing down the driving, as is done in the prior art, conduction losses would occur and they would detract significantly from the overall efficiency of the regulator.

Claims

1. A switching voltage regulator incorporating a driver circuit of a MOS power switch, **characterized in that** said MOS switch is formed of a plurality (n) of power transistors (M1, M2, ..., Mn) connected in parallel to each other.

2. A voltage regulator according to Claim 1, **characterized in that** the first (M1) in said plurality of transistors (M1, M2, ..., Mn) has a larger size (W1) than the other transistors.

3. A voltage regulator according to Claim 1, **characterized in that** the sizes (Wi) of the individual power transistors (M1, M2, ..., Mn) are scaled down (W1 * W2 ≥ W3...≥ Wn).

4. A voltage regulator according to Claim 1, **characterized in that** the sizes (Wi) of the individual power transistors (M1, M2, ..., Mn) are scaled down such that:

$$Wtot = \Sigma_d^n Wn.$$

5. A voltage regulator according to Claim 1, **charac-**

terized in that the first (M1) of said plurality of transistors (M1, M2, ..., Mn) is directly driven directly from said driver circuit (2), while the other translators (M2, ...; Mn) are driven through respective control circuital portions (4, 5, 6,...) connected between the output of the driver circuit (2) and each respective gate terminal of the corresponding transistor.

6. A voltage regulator according to Claim 6, **characterized in that** said control circuital portions (4, 5, 6, ...) are delay blocks.

7. A voltage regulator according to Claim 6, **characterized in that** the transistors (M1 ..., Mn) of said plurality are aranged in a decreasing order of transconductance.

8. A voltage regulator according to Claim 1, **characterized in that** the transistors (M1, ..., Mn) of said plurality are all of the same N-channel or P-channel type.

9. A voltage regulator according to Claim 1, **characterized in that** it comprises a pair of transistors (M1, M2) only, of which the first (M1) is n times larger than the other (M2).

10. A voltage regulator according to Claim 9, **characterized in that** an RC delay block is connected across the gate terminals of said transistor pair (M1, M2).

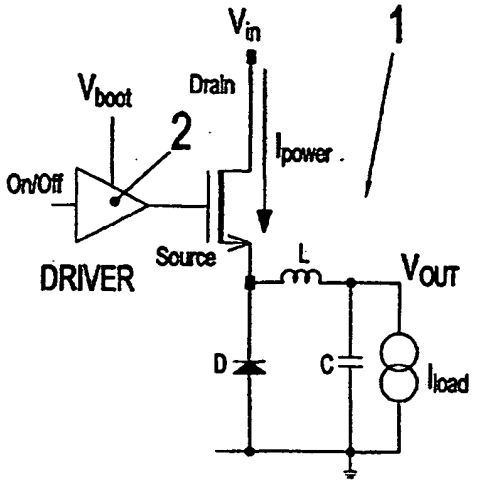


FIG. 1

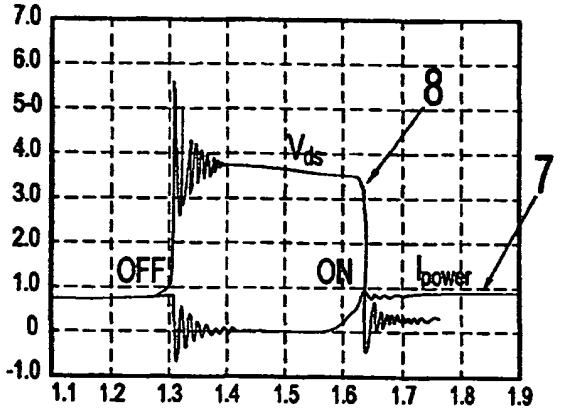


FIG. 1A

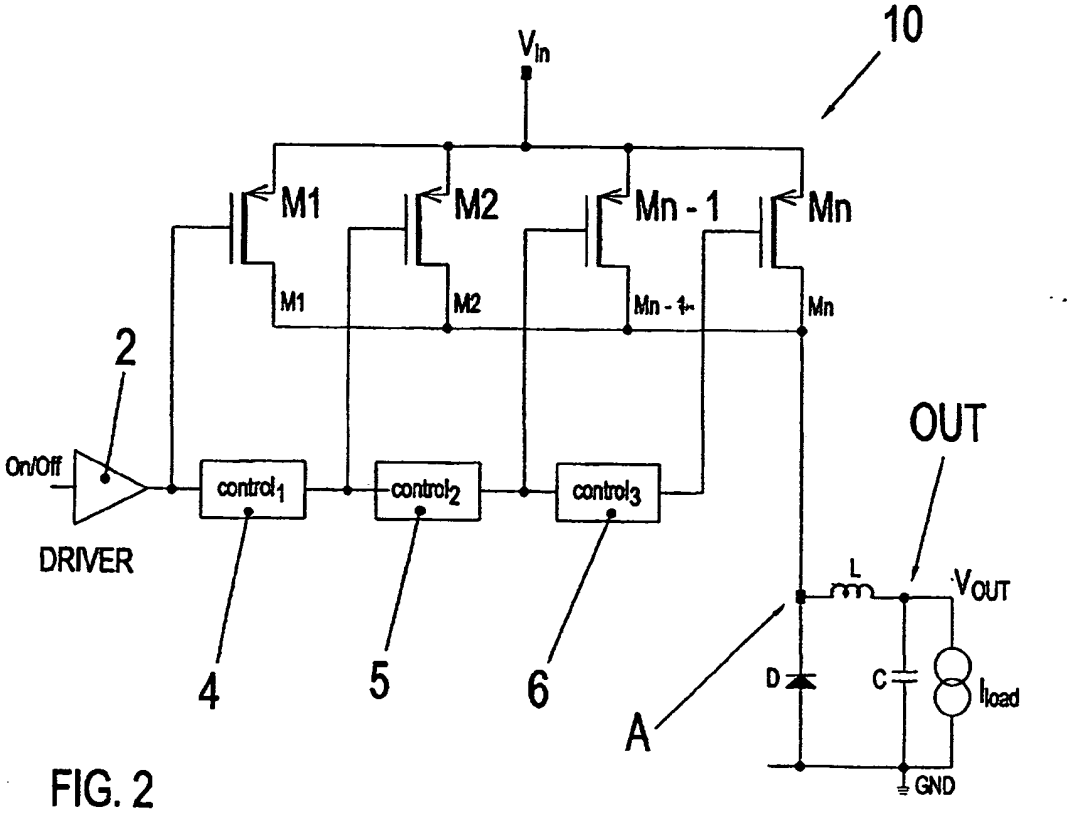
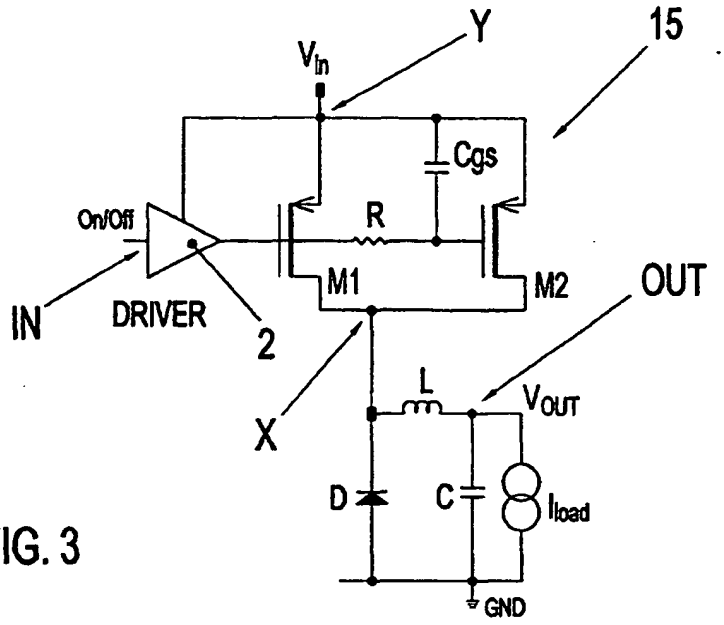


FIG. 2


Y
15
V_{in}
Cgs
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M1
M2
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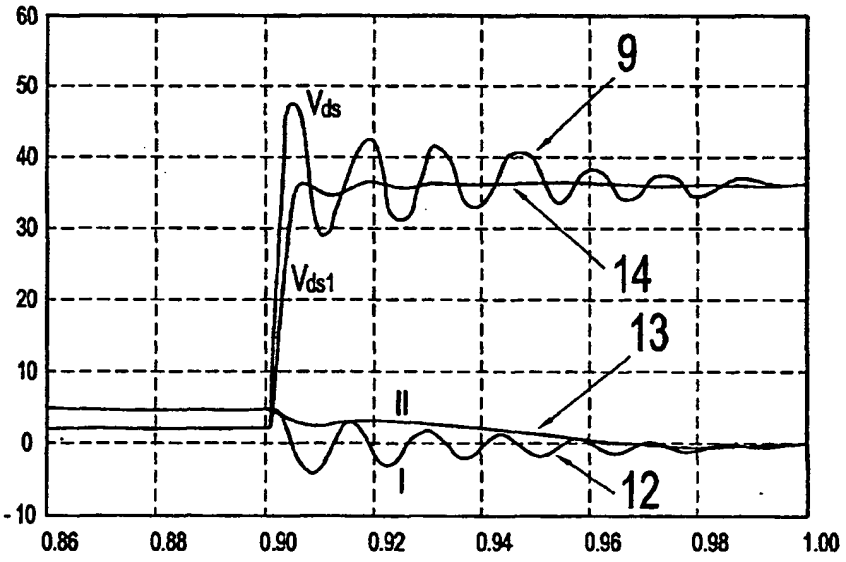
FIG. 3


60
50
40
30
20
10
0
-10
0.86
0.88
0.90
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0.98
1.00
9
V_{ds}
14
V_{ds1}
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II
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12

FIG. 4

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EUROPEAN SEARCH REPORT

Application Number
EP 00 83 0481

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
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X	US 4 616 142 A (UPADHYAY ANAND K ET AL) 7 October 1986 (1986-10-07) * abstract; figures 1-5 *	1	
X	EP 0 581 016 A (KOLLMORGEN CORP) 2 February 1994 (1994-02-02) * abstract; figure 1 *	1	
A	US 5 949 158 A (SCHULZ DETLEF) 7 September 1999 (1999-09-07) * column 4, line 46 - line 65; figure 1 *	1-10	
			TECHNICAL FIELDS SEARCHED (Int.Cl.7) H02M

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	21 November 2000	Gentili, L

CATEGORY OF CITED DOCUMENTS

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